CE4940 WINTER 2016-2017 HOMEWORK HW5

1. **Design** an RTL inverter with VOL = 0.5V if the fabrication process is ON Semi C5 0.5U CMOS. Refer to the course website for the transistor model. **Assume** that all resistances in the design will be fixed at 10KΩ and all lengths are fixed at 0.5U. **Simulate** to verify both voltage and time domain behaviors.
2. **Calculate** the non-saturation region current that flows in the inverter of problem 1. **Use** that current along with the VOL voltage to calculate the channel power P_{NMOS}.
3. **Modify** your SPICE input file so that it produces a table of channel current through time. SPICE can "print" values into the output file accessed through the icons or through the "view" menu. SPICE can print current through two-terminal devices. Thus, since the transistor is not a two terminal device, ask SPICE to print the DC current flowing in the resistor. The spice deck command is **.PRINT DC I(R1)**. Then, check your output file and verify your calculation from problem 2.
4. **Use** the reference inverter and channel width scaling rules to implement the carry out logic function for a full column addition: COUT = AB + AC + BC. **Hint:** factorization removes a transistor in the complex logic. **Hint**: complex logic is followed by an inverter to remove the natural complement behavior. **Simulate** to verify voltage and time domain behavior.

You may submit either paper solution or PDF to the instructor. Your submission packet is due by Wednesday at 5 p.m. in Week 6.